



8Mx72 bits

Unbuffered DDR SDRAM SO-DIMM

HYMD18M725A(L)6-K/H/L

DESCRIPTION

Hynix HYMD18M725A(L)6-K/H/L series is unbuffered 200-pin double data rate Synchronous DRAM Small Outline Dual In-Line Memory Modules (SO-DIMMs) which are organized as 8Mx72 high-speed memory arrays. Hynix HYMD18M725A(L)6-K/H/L series consists of five 8Mx16 DDR SDRAM in 400mil TSOP II packages on a 200pin glass-epoxy substrate. Hynix HYMD18M725A(L)6-K/H/L series provide a high performance 8-byte interface in 67.60mmX 31.75mm form factor of industry standard. It is suitable for easy interchange and addition.

Hynix HYMD18M725A(L)6-K/H/L series is designed for high speed of up to 133MHz and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMD18M725A(L)6-K/H/L series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 64MB (8M x 72) Unbuffered DDR SO-DIMM ECC-based on 8Mx16 DDR SDRAM
- JEDEC Standard 200-pin small outline dual in-line memory module (SO-DIMM)
- 2.5V +/- 0.2V VDD and VDDQ Power supply
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock operations (CK & /CK) with 100MHz/125MHz/133MHz
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ), Data strobes and Write masks latched on both rising and falling edges of the clock
- Data inputs on DQS centers when write (centered DQ)
- Data strobes synchronized with output data for read and input data for write
- Programmable CAS Latency 2 / 2.5 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Interface	Form Factor
HYMD18M725A(L)6-K	VDD=2.5V VDDQ=2.5V	133MHz(*DDR266A)	SSTL_2	200pin Unbuffered SO-DIMM 67.6mm x 31.75mm x 1mm
HYMD18M725A(L)6-H		133MHz (*DDR266B)		
HYMD18M725A(L)6-L		100MHz (*DDR200)		

* JEDEC Defined Specifications compliant

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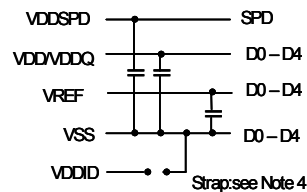
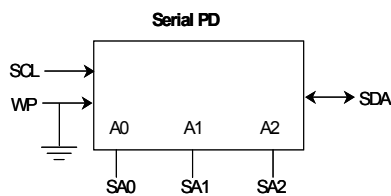
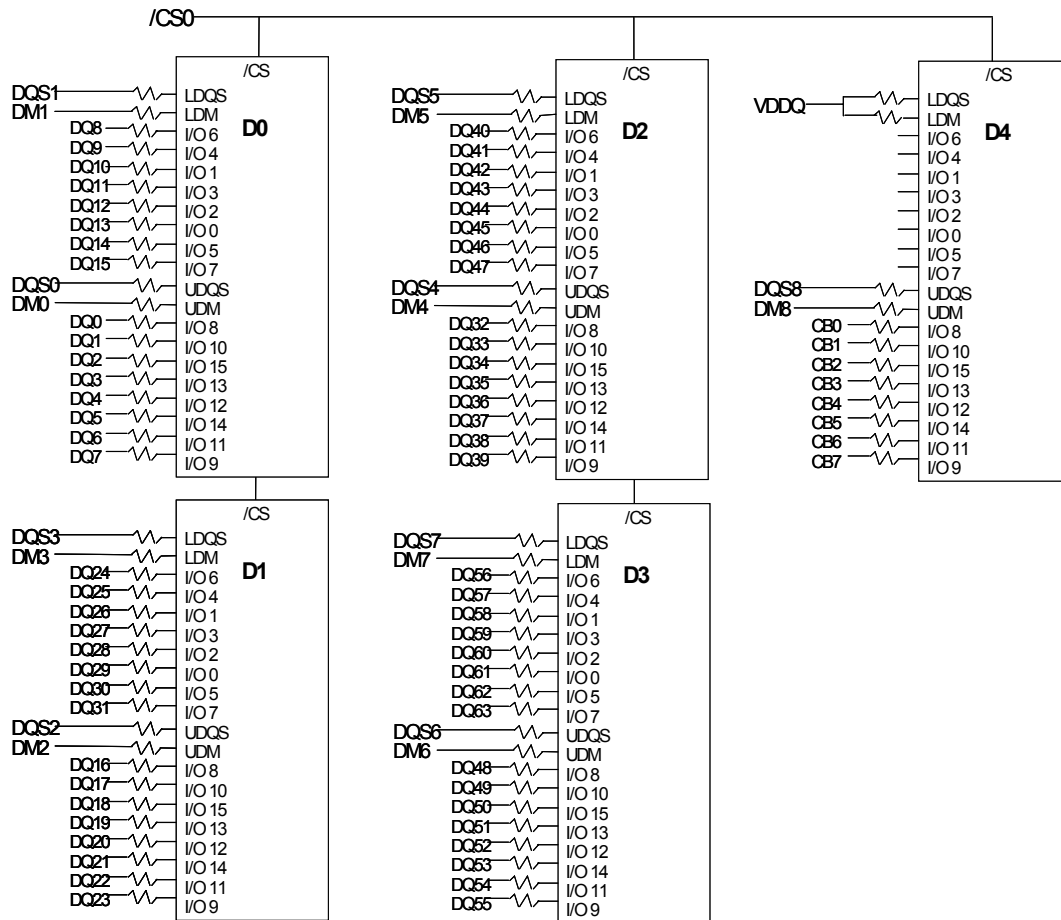
PIN DESCRIPTION

Pin	Pin Description	Pin	Pin Description
CK0, /CK0, CK1, /CK1	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0	Chip Select Input	VSS	Ground
CKE0	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Command Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A11	Address	SA0~SA2	E ² PROM Address Inputs
BA0, BA1	Bank Address	SCL	E ² PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E ² PROM Data I/O
CB0~CB7	Check Bit	WP	Write Protect Flag
DQS0~DQS8	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~DM8	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	/CK1
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	/RAS	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS6	170	DM6
21	VDD	22	VDD	71	CB0	72	CB4	121	/CS0	122	NC	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	DU	124	DU	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	DU	135	DQ34	136	DQ38	185	VSS	186	VSS
37	/CK0	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	NC	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	NC	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	NC	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	NC	98	DU	147	DQS5	148	DM5	197	VDDSPD	198	SA2
49	DQ18	50	DQ22	99	NC	100	A11	149	VSS	150	VSS	199	VDDID	200	DU

FUNCTIONAL BLOCK DIAGRAM



- BA0-BA1 → BA0-BA1 : SDRAMs D0 - D4
- A0 - A11 → A0 - A11 : SDRAMs D0 - D4
- /RAS → /RAS : SDRAMs D0 - D4
- /CAS → /CAS : SDRAMs D0 - D4
- CKE0 → CKE : SDRAMs D0 - D4
- /WE → /WE : SDRAMs D0 - D4

Notes:
 DQ wiring may differ from that described in this drawing, however DQ/DM/DQS relationships are maintained as shown.
 VDDID strap connections
 (for memory device VDD, VDDQ) :
 Strap out (open) : VDD=VDDQ
 Strap In (Vss) : VDD ≠ VDDQ

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	8	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	2.7	V	
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	1.15	1.25	1.35	V	3

Note :

1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5 ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :

1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of V IX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

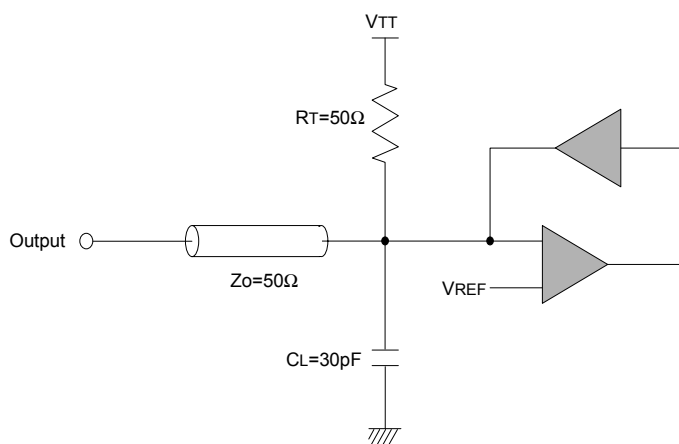
CAPACITANCE (TA=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A11, BA0, BA1	CIN1	31	41	pF
Input Capacitance	/RAS, /CAS, /WE	CIN2	31	41	pF
Input Capacitance	CKE0, CKE1	CIN3	31	41	pF
Input Capacitance	/CS0, /CS1	CIN4	31	41	pF
Input Capacitance	CK0, /CK0, CK1, /CK1	CIN5	17	21	pF
Input Capacitance	DM0 ~ DM7	CIN6	7	10	pF
Data Input / Output Capacitance	DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	10	pF

Note :

1. VDD = min. to max., VDDQ = 2.3V to 2.7V, VODC = VDDQ/2, V_opeak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter		Symbol	Min.	Max	Unit	Note
Input Leakage Current	CMD, Add, /CKE, /CS	ILI	-10	10	uA	1
	CK0, /CK0, CK1, /CK1		-8	8		
	CK2, /CK2		0	0		
Output Leakage Current		ILO	-5	5	uA	2
Output High Voltage		VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage		VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note :

1. VIN = 0 to 3.6V, All other pins are not tested under VIN = 0V
2. DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Test Condition	Speed			Unit	Note
			-K	-H	-L		
Operating Current	IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min) ; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	750	750	700	mA	
Operating Current	IDD1	One bank; Active - Read - Precharge ; Burst Length=2; tRC=tRC(min); tCK=tCK(min) ; address and control inputs changing once per clock cycle	750	750	700	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode ; CKE=Low, tCK= tCK(min)	100			mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS, and DM	200		175	mA	
Active Power Down Standby Current	IDD3P	One bank active ; Power down mode ; CKE=Low, tCK=tCK(min)	125			mA	
Active Standby Current	IDD3N	/CS= HIGH; CKE=HIGH; One bank; Active-Precharge; tRC = tRAS(max); tCK= tCK(min); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	350		250	mA	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOU=0mA	1000	1000	900	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM, and DQS inputs changing twice per clock cycle	1250	1250	1150		
Auto Refresh Current	IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1100	1100	1000		
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min)	Normal	10		mA	
			Low Power	5		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	1625		1500	mA	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-K(DDR266A)		-H(DDR266B)		-L(DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row Cycle Time		tRC	65	-	65	-	70	-	ns	
Auto Refresh Row Cycle Time		tRFC	75	-	75	-	80	-	ns	
Row Active Time		tRAS	45	120K	45	120K	50	120k	ns	
Active to Read with Auto Precharge Delay		tRAP	20	-	20	-	20	-	ns	16
Row Address to Column Address Delay		tRCD	20	-	20	-	20	-	ns	
Row Active to Row Active Delay		tRRD	15	-	15	-	15	-	ns	
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	CK	
Row Precharge Time		tRP	20	-	20	-	20	-	ns	
Write Recovery Time		tWR	15	-	15	-	15	-	ns	
Write to Read Command Delay		tWTR	1	-	1	-	1	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	$\frac{tWR}{tCK} + \frac{tRP}{tCK}$	-	$\frac{tWR}{tCK} + \frac{tRP}{tCK}$	-	$\frac{tWR}{tCK} + \frac{tRP}{tCK}$	-	CK	15
System Clock Cycle Time	CL = 2.5	tCK	7.5	12	7.5	12	8.0	12	ns	
	CL = 2		7.5	12	10	12	10	12	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.5	-	0.5	-	0.6	ns	
Data-Out hold time from DQS		tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	1, 10
Clock Half Period		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns	1,9
Data Hold Skew Factor		tQHS	-	0.75	-	0.75	-	0.75	ns	10
Valid Data Output Window		tDV	tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		ns	
Data-out high-impedance window from CK, /CK		tHZ	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	17
Data-out low-impedance window from CK, /CK		tLZ	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	17
Input Setup Time (fast slew rate)		tIS	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		tIH	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		tIS	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		tIH	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Pulse Width		tIPW	2.2		2.2		2.5	-	ns	6

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

- continued -

Parameter	Symbol	-K(DDR266A)		-H(DDR266B)		-L(DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	0.35	-	CK	
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	0.35	-	CK	
Clock to First Rising edge of DQS-In	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	CK	
Data-In Setup Time to DQS-In (DQ & DM)	tDS	0.5	-	0.5	-	0.6	-	ns	6,7, 11~13
Data-in Hold Time to DQS-In (DQ & DM)	tDH	0.5	-	0.5	-	0.6	-	ns	
DQ & DM Input Pulse Width	tDIPW	1.75	-	1.75	-	2	-	ns	
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	0	-	CK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	2	-	CK	
Exit Self Refresh to Any Execute Command	tXSC	200	-	200	-	200	-	CK	8
Average Periodic Refresh Interval	tREFI	-	15.6	-	15.6	-	15.6	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE.
3. For command/address input slew rate $\geq 1.0V/ns$
4. For command/address input slew rate $\geq 0.5V/ns$ and $< 1.0V/ns$
This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tIS	Delta tIH
V/ns	ps	ps
0.5	0	0
0.4	+50	0
0.3	+100	0

5. CK, /CK slew rates are $\geq 1.0V/ns$
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation
7. Data latched at both rising and falling edges of Data Strokes(LDQS/UDQS) : DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)

10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQ max, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.

Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tDS	Delta tDH
V/ns	ps	ps
0.5	0	0
0.4	+75	+75
0.3	+150	+150

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

I/O Input Level	Delta tDS	Delta tDH
mV	ps	ps
+280	+50	+50

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as $(1/\text{SlewRate1}) - (1/\text{SlewRate2})$. For example, if slew rate 1 = 0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

$(1/\text{SlewRate1}) - (1/\text{SlewRate2})$	Delta tDS	Delta tDH
ns/V	ps	ps
0	0	0
+/-0.25	+50	+50
+/- 0.5	+100	+100

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

15. $tDAL = (tWR / tCK) + (tRP / tCK)$. For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.

Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,

$$tDAL = (15 \text{ ns} / 7.5 \text{ ns}) + (20 \text{ ns} / 7.5 \text{ ns}) = (2.00) + (2.67)$$

Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clock

16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be $tRAS - BL/2 \times tCK$.

17. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).

SIMPLIFIED COMMAND TRUTH TABLE

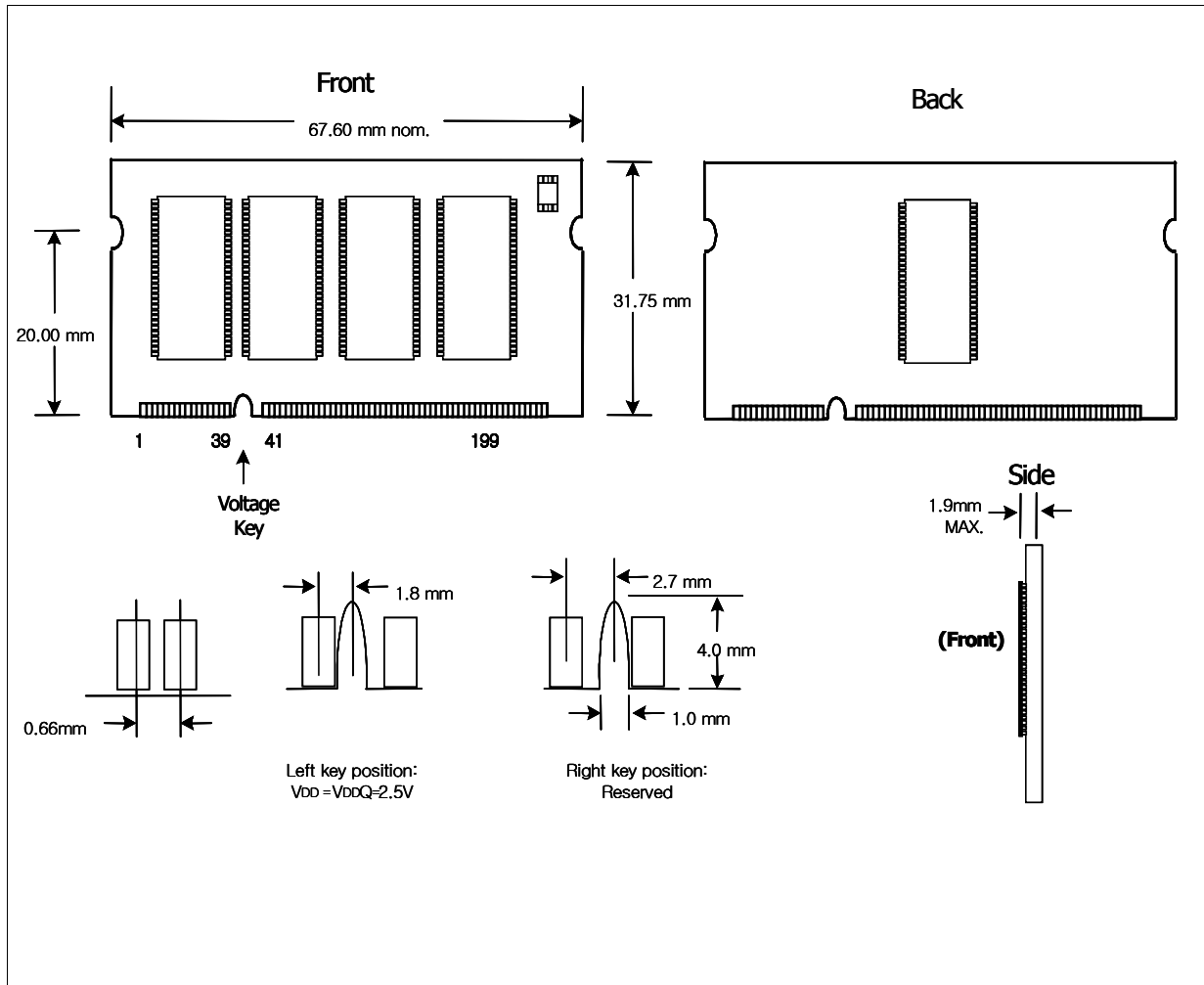
Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode (Clock Suspend)	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

- LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
- OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
- If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+tRP).
- If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechagre delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
- If A10/AP is High when Row Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

PACKAGE DIMENSIONS



SPD SPECIFICATION

(8Mx72 Unbuffered DDR SO-DIMM)

SERIAL PRESENCE DETECT

Bin Sort : K(DDR266A@CL=2), H(DDR266B@CL=2.5),L(DDR200@CL=2)

Byte#	Function Description	Function Supported			Hexa Value			Note
		K	H	L	K	H	L	
0	Number of Bytes written into serial memory at module manufacturer	128 Bytes			80h			
1	Total number of Bytes in SPD device	256 Bytes			08h			
2	Fundamental memory type	DDR SDRAM			07h			
3	Number of row address on this assembly	12			0Ch			1
4	Number of column address on this assembly	9			09h			1
5	Number of physical banks on DIMM	1Bank			01h			
6	Module data width	72 Bits			48h			
7	Module data width (continued)	-			00h			
8	Module voltage Interface levels(VDDQ)	SSTL 2.5V			04h			
9	DDR SDRAM cycle time at CAS Latency=2.5(tCK)	7.5ns	7.5ns	8ns	75h	75h	80h	2
10	DDR SDRAM access time from clock at CL=2.5 (tAC)	+/-0.75ns	+/-0.75ns	+/-0.8ns	75h	75h	80h	2
11	Module configuration type	ECC			02h			
12	Refresh rate and type	15.6us & Self refresh			80h			
13	Primary DDR SDRAM width	x16			10h			
14	Error checking DDR SDRAM data width	x8			08h			
15	Minimum clock delay for back-to-back random column address(tCCD)	1 CLK			01h			
16	Burst lengths supported	2,4,8			0Eh			
17	Number of banks on each DDR SDRAM	4 Banks			04h			
18	CAS latency supported	2, 2.5			0Ch			
19	CS latency	0			01h			
20	WE latency	1			02h			
21	DDR SDRAM module attributes	differential clock input			20h			
22	DDR SDRAM device attributes : General	+/-0.2Voltage tolerance, Concurrent Auto Precharge			40h			
23	DDR SDRAM cycle time at CL=2.0(tCK)	7.5ns	10ns	10ns	75h	A0h	A0h	
24	DDR SDRAM access time from clock at CL=2.0(tAC)	+/-0.75ns	+/-0.75ns	+/-0.8ns	75h	75h	80h	
25	DDR SDRAM cycle time at CL=1.5(tCK)	-			00h			
26	DDR SDRAM access time from clock at CL=1.5(tAC)	-			00h			
27	Minimum row precharge time(tRP)	20ns	20ns	20ns	50h	50h	50h	
28	Minimum row activate to row active delay(tRRD)	15ns	15ns	15ns	3Ch	3Ch	3Ch	
29	Minimum RAS to CAS delay(tRCD)	20ns	20ns	20ns	50h	50h	50h	
30	Minimum active to precharge time(tRAS)	45ns	45ns	50ns	2Dh	2Dh	32h	
31	Module row density	64MB			10h			
32	Command and address signal input setup time(tIS)	0.9ns	0.9ns	1.1ns	90h	90h	B0h	
33	Command and address signal input hold time(tIH)	0.9ns	0.9ns	1.1ns	90h	90h	B0h	
34	Data signal input setup time(tDS)	0.5ns	0.5ns	0.6ns	50h	50h	60h	
35	Data signal input hold time(tDH)	0.5ns	0.5ns	0.6ns	50h	50h	60h	
36~40	Reserved for VCSDRAM	Undefined			00h			
41	Minimum active / auto-refresh Time (tRC)	65ns	65ns	70ns	41h	41h	46h	
42	Minimum auto-refresh to active / auto-refresh command period (tRFC)	75ns	75ns	80ns	4Bh	4Bh	50h	
43	Maximum cycle time (tCK max)	12ns	12ns	12ns	30h	30h	30h	
44	Maximum DQS-DQ skew time (tDQSQ)	0.5ns	0.5ns	0.6ns	32h	32h	3Ch	
45	Maximum read data hold skew factor (tQHS)	0.75ns	0.75ns	0.75ns	75h	75h	75h	
46~61	Superset Information(may be used in future)	Undefined			00h			
62	SPD Revision code	Initial release			00h			
63	Checksum for Bytes 0~62	-			1Dh	48h	E2h	

SERIAL PRESENCE DETECT(continued)

Byte#	Function Description	Function Supported			Hexa Value			Note
		K	H	L	K	H	L	
64	Manufacturer JEDEC ID Code	Hynix JEDEC ID			ADh			
65~71	----- Manufacturer JEDEC ID Code	-			00h			
72	Manufacturing location	Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area			0*h 1*h 2*h 3*h 4*h 5*h			6
73	Manufacture part number(Hynix Memory Module)	H			48h			
74	----- Manufacture part number(Hynix Memory Module)	Y			59h			
75	----- Manufacture part number(Hynix Memory Module)	M			4Dh			
76	Manufacture part number (DDR SDRAM)	D			44h			
77	Manufacture part number(Memory density)	1			31h			
78	Manufacture part number(Module Depth)	8			38h			
79	Manufacture part number(Module type)	M			4Dh			
80	Manufacture part number(Data width)	7			37h			
81	-----Manufacture part number(Data width)	2			32h			
82	Manufacture part number(Refresh, # of Bank.)	5(4K refresh,4Bank)			35h			
83	Manufacture part number(Component Generation)	A			41h			
84	Manufacture part number(Component configuration)	6			36h			
85	Manufacture part number(Hyphen)	-			2Dh			
86	Manufacture part number(Minimum cycle time)	K	H	L	4Bh	48h	4Ch	
87~91	Manufacture part number(T.B.D)	-			-			
92	Manufacture revision code(for Component)	-			-			
93	Manufacture revision code (for PCB)	-			-			
94	Manufacturing date(Year)	-			-			3
95	Manufacturing date(Week)	-			-			3
96~99	Module serial number	-			-			4
100~128	Manufacturer specific data (may be used in future)	Undefined			00h			5
129~255	Open for customer use	Undefined			00h			5

Note :

1. The bank address is excluded
2. These value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number system
5. These bytes undefined and coded as '00h'
6. Refer to Hynix web site

Byte 83~85, Low Power Part

Byte#	Function Description	Function Supported			Hexa Value			Note
		K	H	L	K	H	L	
83	Manufacture part number(Component Generation)	A			41h			
84	Manufacture part number(Low Power Part)	L			4Ch			
85	Manufacture part number(Component Configuration)	6			36h			